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Modified Series-Parallel Switched Capacitor with Adjustable Equilibrium Setpoint for Pack-to-Multicells Battery Voltage Equalization Circuit

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Abstract. Voltage unbalance is one problem on series-connected battery pack. Different circuit strategies has been developed to overcome the issue by presenting dissipative or nondissipative mechanisms to achieve state of charge equalization of the battery. The presented strategy in this paper uses a special series-parallel structure of switched capacitor with the modification of additional equilibrium voltage setpoint adjustment. The proposed design is able to push the final averaged voltage (3.79 V) higher than conventiional series-parallel structure (3.70 V).

Keywords: *battery management system; pack-to-multicells; series-parallel structure; switched capacitor; voltage equalization.*

1 Introduction

Rechargeable Lithium battery pack requires control to stabilize its operation. Battery management system (BMS) is an integrated electronic devices specially designed to monitor and protect the batteries from any abnormal conditions, e.g., overcharged, over discharged, overcurrent, overtemperature, etc. Hence, there are several parameters that need to be measured or estimated, e.g., voltage, current, temperature, state of charge (SOC), state of health (SOH), etc [1-3]. The SOC represents how many percentage of remaining useful capacity of a cell compared to its nominal capacity. SOC cannot be measured directly but can be correlated with battery voltage. Unbalanced SOC will reduce the total cycle time [3].

In general, there are two equalization circuit mechanism to balance the SOC of the battery pack: passive or active [4]. In passive mechanism, the controllable shunt resistor used to dissipate excessive energy on high SOC cells [5]. In active mechanism, the excessive energy of the high SOC cells is transfered to low SOC cells by using specialized nondissipative equalization circuit, e.g., switched capacitor [3,6-10], multiwinding transformer [9], etc. It is obvious that the main advantages of active equalization circuit design is high efficiency [11-12].

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However, the equalization speed depends on switches structures because the energy source and receiver can be either a single cell or an entire battery pack.

The proposed equalization circuit structure in this paper is focused on switched-capacitor (SC) based circuit design. The main advantages of capacitor is low-cost component and responsive voltage characteristics. The latter point refers to the fact that capacitor tends to maintain its voltage so that it will store or discharge some energy in form of electric field if external voltage is higher or lower than its voltage, respectively. Adjacent cell-to-cell (ACTC) is one of the first SC-based equalization topology used in history [6]. The SC circuits in ACTC topology are used to balance the voltage of adjacent cell only. To improve the overall voltage equalization speed in long series-connected battery pack, some modifications have been conducted to deliver direct energy transfer path by using, for example, chain [7], multi-tiered [8], modularized [9], shared [3], and series-parallel [10] SC structures. Chain SC structure simply add one SC circuit to balance the voltage between first and last cells in battery string, while multi-tiered SC structure add several SC circuits to balance between cells in any determined location. However, the number of SC circuits and the switching complexity in multi-tiered structure may not feasible for some limited space of battery applications. Modularized SC structure can reduces the number of required SC by dividing long battery pack into several modules then there is voltage equalization on both inside module and inter-module. Shared SC structure used only one SC circuit but only one cell at a time that can be equalized directly in either single-cell-to-single-cell (SCTSC), single-cell-to-pack (SCTP), or pack-to-single-cell (PTSC) operation mode.

The study in this paper is motivated by one clever SC structure, i.e., series-parallel structure as developed by [10]. The idea is using capacitors to follow the voltage of their corresponding cell at a time, then compare their voltage to achieve average voltage at another time in respectable short period. So, everytime the capacitor is in parallel with the cell, the individual cells voltage on battery pack will also tend to be equalized into average value, simultaneously. In this paper, the proposed design modifies series-parallel SC structure by using additional stepdown dc-dc converter whose output will determine the setpoint or target of the final equalization voltage value. It is operated in pack-to-multicells (PTMC) mode to enhance the equalization speed compared to PTSC mode.

2 System Description

The basic circuit schematic of the proposed series-parallel SC structure design is presented in Fig.1. There are n cells with same chemical material connected in series configuration of battery pack. Each individual cell is connected in parallel to single switched capacitor with both positive and negative path is controlled so

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that will be no short circuit failure. Those are the basic part of series-parallel SC equalization described by [10]. In this paper, there is some modification to achieve customized equalization voltage setpoint by using a step down dc-dc converter as a voltage source on some specified value.

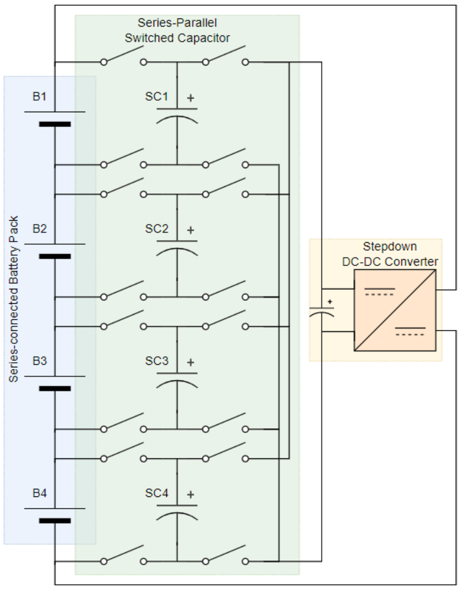

Figure 1 Basic circuit schematic of the proposed design.

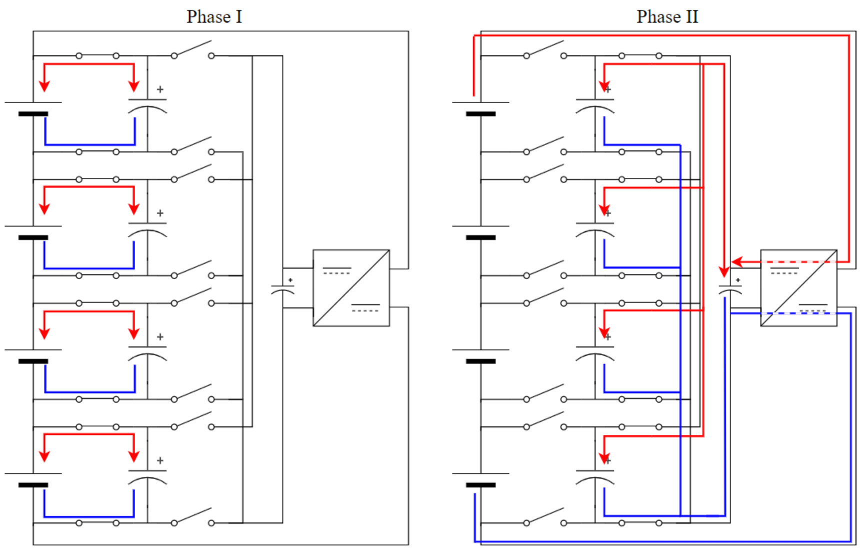

Figure 2 Energy flow in two equalization phases.

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The mechanism of equalization by the proposed series-parallel SC circuit design is illustrated by Fig.2. There is two phases of equalization. At phase I, capacitors are connected in parallel with their corresponding battery cells. The capacitors themselves are connected in series just like the battery pack configuration itself. The voltage of individual capacitor is trying to follow the cell voltage. The outer switches are opened and must be ensured to isolate positive and negative nodes of one cell from anothers.

At phase II, capacitors are disconnected from their corresponding battery cells and then their positive and negative nodes are now connected with each other as if they are parallel-connected. Hence the name series-parallel is referred to. Now, the inner switches are opened and must be ensured to isolate positive and negative nodes of one cell from anothers. The capacitors will try to share their charge until they reach the same voltage value. The dc-dc converter acts as a voltage source to set the final voltage of each capacitor. The output current of dc-dc converter may be limited by some specified value so there is no excessive transient current spike at the transition from phase I to phase II.

After phase II, the capacitors are in phase I again and the cycle is continued. The proposed series-parallel SC structure acts as an energy distributor from pack via dc-dc converter into every cells in simultaneous fashion. The capacitance value of each capacitor may be small so their voltage response is fast enough on each equalization phase, but not too fast so the charge equalization is not too small. The switching period must be considered based on this capacitance value. On the other hand, the output impedance of dc-dc converter must be small enough so it cannot drop to lower voltage and push the final individual cell voltage as high as possible. To achieve this, a supercapacitor may be used as a voltage buffer on the dc-dc converter output side.

3 Experiment Setup

The study of the proposed design in this research will be performed through some simulation. The software used to simulate the circuit behavior is Simscape from Matlab™ 2021a. Equalization performance of the proposed series-parallel SC design will be compared to the conventional design as in [10] and to the shared SC structure with PTSC operational mode because of the structure similiarity.

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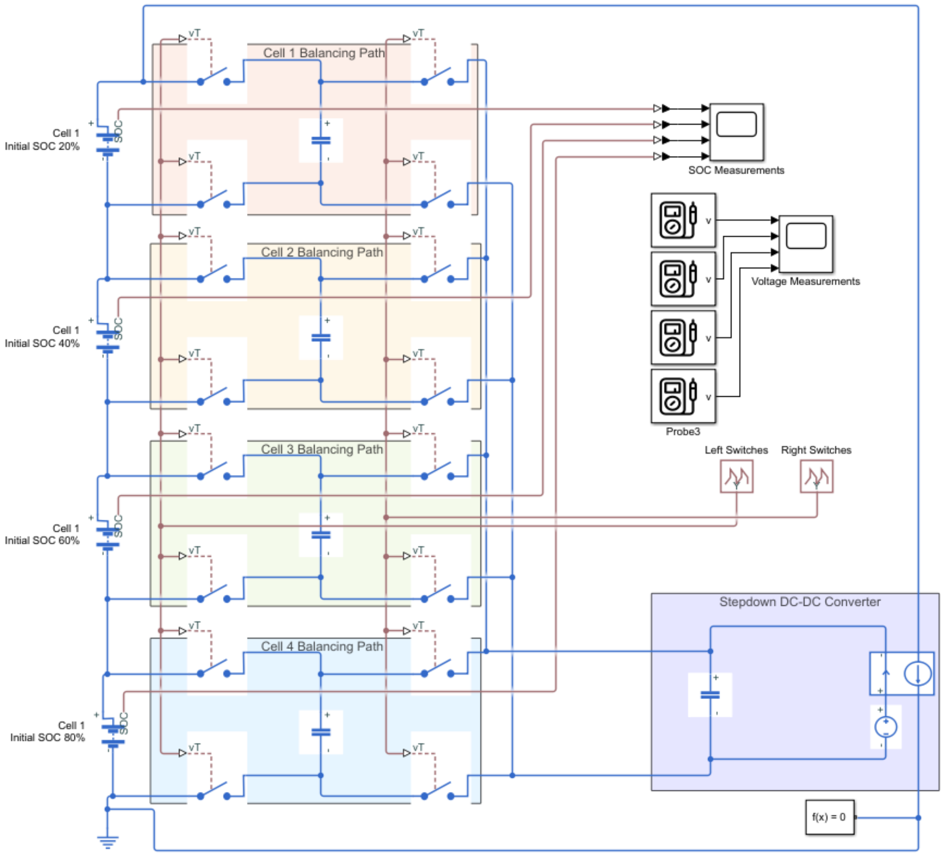

Figure 3 Schematic modeling of the proposed design in Simscape^{TM}.

The battery model parameter in the simulation will be based on real life data of LG HG2 cylindrical Lithium-NMC battery as an example. However, its nominal capacity (3000 mAh) will be reduced by the factor of 300 to speed up the stop time of computation and save the memory. The capacitor is modeled with some equivalent series resistance (ESR). Low ESR and high capacitance value in the modeled capacitor is prefered to achieve low dissipation losses and low switch frequency so it can be simulated with large step time and low memory. In reality, low frequency switching may be useful to reduce wear out and degradation for mechanical relay.

In conventional series-parallel SC structure, there is no dc-dc converter. In the proposed series-parallel SC structure, dc-dc converter is modeled as a voltage source set to be high voltage limit of cell (4.2 Volt) and then the current extracted by the output determines the current extracted from the input (i.e. the pack) by current ratio of 100% step down converter. The switches in every equalization

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path for both conventional and modified SC are operated in synchronous manner. Meanwhile, shared SC structure in PTSC mode has similar structure with the proposed series-parallel SC, except that the SC section is used once in order to provide isolated power line between the nonisolated dc-dc converter and any floating target [3]. Shared SC structure in PTSC mode use selector switches circuit which is normally open and only connected on one cell at a time whose the SOC or voltage is the lowest.

Table 1 List of simulation component parameters.

No	Name of Components	General Type of Components	Parameter Values
1	Battery	Li-NMC	Test data of an LG HG2 sample; Nom.Cap. = 3Ah / 300
2	Capacitor	Low ESR	C = 10 mF; R = 0.1 Ω
3	Switch	Electromechanical Relay	R_{on} = 0.1 Ω; R_{off} = 1 MΩ; %Duty= 50%; T_{rise} = T_{fall} = 0.01s
4	DC-DC Converter	Stepdown	CV setpoint = 4.2 V
5	Storage Capacitor	Supercapacitor	C = 1 F; R = 10 Ω

4 Results and Analysis

The study consider three SC-based equalization circuits: 1. Shared SC structure with PTSC mode as in [3]; 2. Conventional series-parallel SC structure as in [10]; 3. Modified series-parallel SC structure, which is the proposed design. The first circuit is chosen as a comparison to study whether the equalization speed of the proposed PTMC design can achieve faster performance than PTSC mode of the shared SC structure. Fig.4 shows that the PTSC still win the speed performance (179.44 s) while the proposed PTMC design (558.24 s) even slower than the equalization time of the conventional series-parallel design (402.15 s). However, if the number of cells in series-connected battery pack is much larger, the PTSC will getting hard to balance the group of lowest voltage cells. Furthermore, the selector switches is triggered between on and off very frequently so the risk of early wear out will getting increased. The simulation on larger number of cells has not been conducted in this study because of the computational issue. Further validation will be performed in the future by some prototype testing methods.

The conventional series-parallel SC structure is also chosen as a comparison to study whether there is performance improvisation by modifying the circuit with additional step down dc-dc converter. The simulation results in also shows that the final voltage deviation (3.5 mV) and averaged cells voltage (3.7973 V) are better than the conventional design whose deviation is only slightly different (3.8 mV) but final averaged cells voltage is significant (3.7037 V). However, this improvement can be biased by higher fluctuation of cells voltage in the proposed design. If that is true, slight equalized voltage performance between both series-

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parallel SC may be differentiated by testing the effect of different external current variation. The fluctuation on the simulation may seems exaggerated because the cell parameters are not all adjusted, only the nominal capacity is. Hence again, the further experiment validation need to be considered.

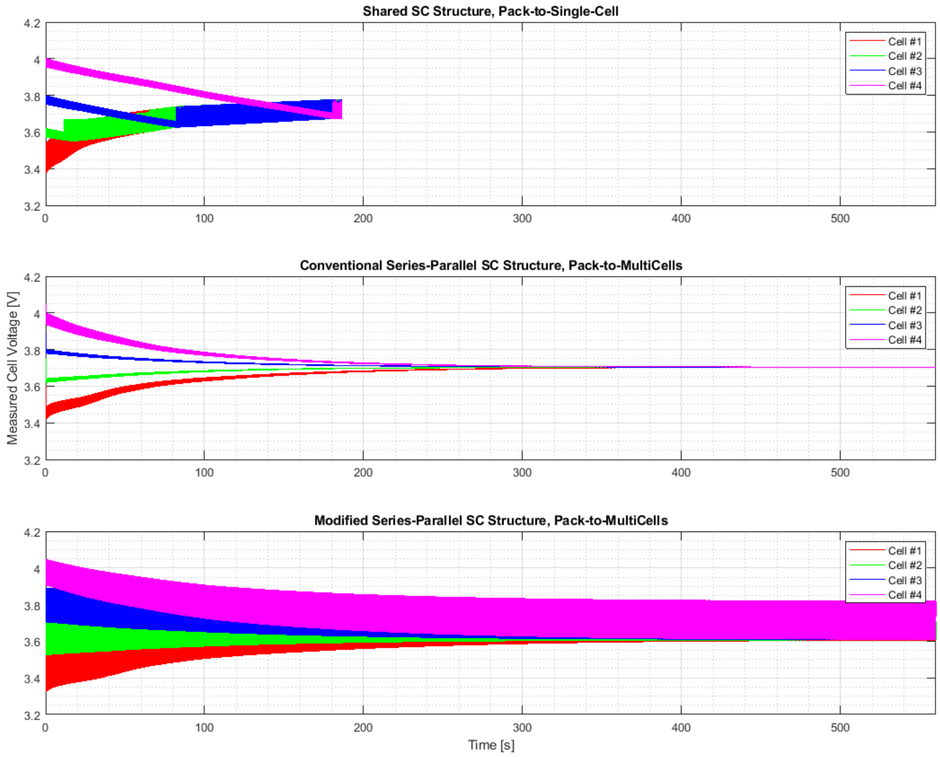

Figure 4 Simulation results of different voltage equalization circuit.

5 Conclusion

The proposed series-parallel SC structure with adjustable equilibrium voltage has been simulated in Simscape™, compared with the conventional series-parallel SC structure and shared SC structure in PTSC mode because of their similarity. The proposed design is advantaged from the shared SC design by avoiding early degradation on any switches. The final equalized voltage value of the proposed design is observed to be larger than the conventional series-parallel SC design. However, the overemphasized voltage fluctuation and expensive computational issue limits the study based on simulation methods. Further theoretical analysis will be developed. Some prototype circuit testing will also be conducted in the future research to validate the simulation results of the proposed design.

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